Journal of Academia and Industrial Research (JAIR)
Volume 2, Issue 11 April 2014

ISSN: 2278-5213

RESEARCH ARTICLE

Performance Analysis of Loop Frame of Reference over Bus Frame of Reference

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Abstract

Performance analysis of loop frame of reference over bus frame of reference is carried out in this study. Impedance matrices for fault current calculations are found out in bus and loop frames of references. In bus frame of reference, bus impedance matrix Z_{bus} is formulated by inverting bus admittance matrix Y_{bus}. In loop frame of reference, loop impedance matrix Z_{loop} is calculated using graph theory. These methods are compared and verified with the standard IEEE 14 bus system. The results have proved that loop frame of reference can outperform the bus frame of reference with less computation time and memory. This performance analysis can be applied for fault analysis of larger power system networks.

Keywords: Circuit analysis, graph theory, bus frame, loop frame, fault analysis, power system networks.

Introduction

One of the reasons for the recent interests in graph theory is its applicability in many diverse areas of power system engineering. It can be applied to different sections which include modeling and analysis. The formulation of suitable mathematical model is the first step of solving an electrical network. The model must describe the characteristics of individual network components and the relationship that govern the interconnection of these elements. The form of network matrix used in the performance equation depends on the frame of reference, namely bus or loop. In bus frame of reference, the variables are nodal voltages and nodal currents. In loop frame of reference, the variables are loop voltages and loop currents. To describe the geometrical structure of a network, it is sufficient to replace the network components by single line segments (primitive elements) and their terminals (nodes).

The bus frame of reference in admittance form (Y_{bus}) was employed in the first application of digital computers for short circuit studies. A complete iterative solution for each fault type and fault locations was required. The currents and voltages were also required for large number of fault locations. Consequently, this method was not adopted generally. The development of techniques for applying digital computer to form the bus impedance matrix (Z_{bus}) made it feasible to use Thevenin's theorem for short circuit calculations. This approach provided an efficient means of determining short circuit current and voltage because these values could be obtained with few arithmetic operations involving only related portions of the bus impedance matrix (Gonzalez, 2007; Wang *et al.,* 2010; Sarkar *et al*., 2011; Oepomo, 2012). But, there are other important considerations such as computer memory utilization to store the impedance matrix.

In the nodal reference frame, the network is modeled by voltages at each node and current injections into each node within the network. In contrast, the loop reference frame is modeled by the voltages and currents around each loop formed within the network. Network behavior is characterized by the flows within each assigned loop. In either case, formation of network equations is dependent on the frame of reference adopted. Use of the nodal reference frame is widely accepted. Despite this, the nodal frame of reference can only provide information for a node within the network. It is not able to provide any indication about the distribution of power flow contributed by different sources through the network.

Network equations can be established either in the bus frame of reference (using Z_{bus}) or in the loop frame of reference (using Z_{loop}) for mathematical modeling of power system. The mathematical calculations involved are difficult to perform by hand. The calculations can be easily done by computer programming. In practical application, Z_{bus} is more common than Z_{loop} analysis. If the size of the matrix is of great concern in terms of reduction of the required memory to be stored during fault studies, then Z_{loop} can gain some benefits. If the original power network has 'n' nodes and 'b' branches, then the number of linearly independent current and voltage law equations is (b-n+1). The size of the Z_{loop} matrix is (b-n+1) by (b-n+1); so, the size of the Z_{bus} matrix is (n-1) by (n-1) for the same power network. It can be concluded that if (n-1) is bigger than (b-n+1) then the size of the Z_{bus} matrix is bigger than the size of the Z_{loop} matrix. It should be apparent that computer using either a loop or a bus matrix technique may solve power system faults (Brameller and Pandey, 1974; Wang *et al.,* 2007; Bi *et al*., 2008; Shirinivas *et al*., 2010).

In this study, bus impedance matrix Z_{bus} has been formulated by inverting bus admittance matrix (Y_{bus}). Graph theory has been used to find loop impedance matrix Z_{loop}. These methods are applied on standard IEEE 14 bus system using MATLAB programs. The computation time and memory space required are compared for the above two frames of references.

Materials and methods

Impedance matrices in fault calculation: The impedance matrices used in fault analysis are bus impedance matrix and loop impedance matrix. The bus impedance matrix can be used to estimate the fault at any point of the system. Usually this method is useful for large systems. Bus impedance matrix is the inverse of the bus admittance matrix ($Z_{bus=}|Y_{bus}|^{-1}$). The matrix consisting of driving point impedances and transfer impedances of the network is called as bus impedance matrix. Bus impedance matrix can also be formed by building algorithm or using triangular factorization of Y_{bus} matrix. Fault analysis of power system can be carried out with loop frame of reference of graph theory. Fault analysis followed by stability analysis is essential for taking preventive and corrective actions in a power system network (Fan *et al*., 1996; Peponis *et al*., 1996; Ayasun *et al*., 2006). Recently, researchers have analyzed stability of the system using artificial neural network and genetic algorithm based models (Ibrahim and Morcos, 2002; Abdelaziz *et al*., 2006; Barros and Perez, 2006; Sarkar *et al*., 2010). Fault diagnosis has been done using Artificial Intelligence techniques (Sarfi *et al*., 1995; Sivanagaraju *et al*., 2005; Wang *et al.,* 2008; Dong *et al.,* 2008; Zhang *et al*., 2011). Advanced methods like Fuzzy wavelet neural network and WAMS/PMU have also been adopted for fault detection (Ghoudjehbaklo and Danai, 2001; Saiver and Das, 2009; Zhang *et al*., 2010, 2012). The following steps can be followed for fault analysis using impedance matrix in bus frame and loop frame of references.

Step 1: Obtain bus impedance matrix, Z_{bus} by inverting bus admittance matrix, Y_{bus}.

Step 2: Obtain the graph of a standard IEEE 14-bus system replacing the elements by line segments.

Step 3: Consider a tree of the graph and form loops by adding links to every branch of the network.

Step 4: Compute loop incidence matrix '*C*' with basic loops.

Step 5: Form primitive impedance matrix 'Z_{bb}' using line data of the system.

Step 6: Calculate loop impedance as follows
$Z_{loop} = C^{t} * Z_{bb} * C$.

Step 7: Compute the fault currents under bus frame of reference and loop frame of reference and compare the results.

Results and discussion

Network graph for a standard IEEE 14-bus system: One line diagram of a standard IEEE 14-Bus system is shown in Fig. 1 and its graph with links represented by dotted lines is shown in Fig. 2. In this system, apparently all buses are interconnected to form several loops. Basic loops are formed by the addition of links. By selecting appropriate loop, loop incidence matrix can be determined, which is then used to determine loop impedance matrix. The loop impedance matrix can be used for determining fault currents.

Fig. 1. One line diagram of IEEE 14-bus system.

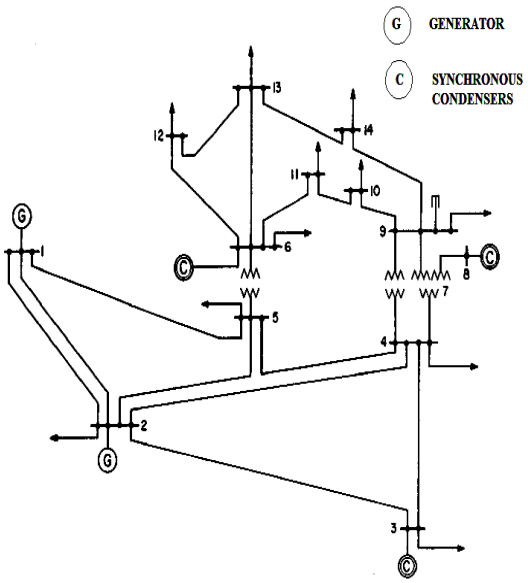


Fig. 2. Graph of an IEEE14-bus system.

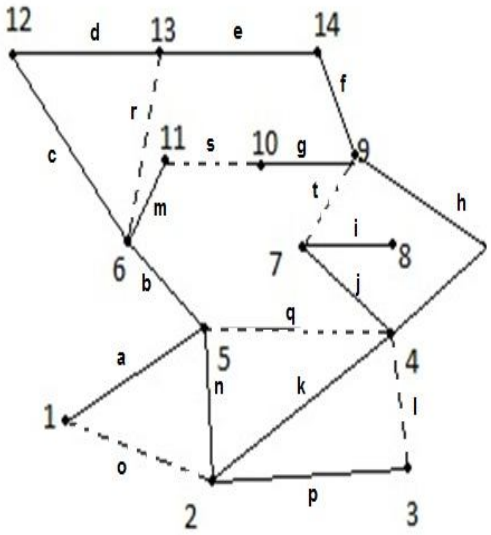


Table 1. Elements of Loop Incidence Matrix 'C'.

Element	Loop					
	l	O	q	r	s	t
a	0	-1	0	0	0	0
b	0	0	0	0	0	0
c	0	0	0	-1	1	0
d	0	0	0	-1	1	0
e	0	0	0	0	1	0
f	0	0	0	0	-1	0
g	0	0	0	0	1	0
h	0	0	0	0	0	-1
i	0	0	0	0	0	1
j	0	0	0	0	0	1
k	-1	0	1	0	0	0
m	0	0	0	0	-1	0
n	0	1	-1	0	0	0
p	1	0	0	0	0	0
l	1	0	0	0	0	0
o	0	1	0	0	0	0
q	0	0	1	0	0	0
r	0	0	0	1	0	0
s	0	0	0	0	1	0
t	0	0	0	0	0	1

Basic loop incidence matrix 'C': Basic loop incidence matrix '*C*' with '*i*' rows and '*j*' columns can be calculated from the incidence of the elements to basic loops of the connected graph. The elements of *C* matrix are found out with the following criterion and are given in Table 1.
Criterion 1: If, i^{th} element is incident to and oriented in same direction as j^{th} basic loop, then C_{ij}=1.
Criterion 2: If, i^{th} element is incident to and oriented in the opposite direction as the j^{th} basic loop, then C_{ij}= -1.
Criterion 3: If, i^{th} element is not incident to j^{th} basic loop, then C_{ij}=0.

Primitive impedance matrix 'Z_{bb}': Primitive impedance matrix comprises of all the line impedance of the network represented by Z_{bb} which is a diagonal matrix in such a way that all the off-diagonal elements are zero. Table 2 represents 20×20 matrix of IEEE14 bus system in which only diagonal elements are tabulated.

Loop impedance matrix 'Z_{loop}': The loop impedance matrix Z_{loop} can be obtained by using the basic loop incidence matrix '*C*' to relate the variables and parameters of loop quantities of the interconnected network. Z_{loop} is calculated by following Step 6. The loop impedance matrix 'Z_{loop}' is given below.

$$\begin{pmatrix} 0.5728 & 0 & -0.1856 & 0 & 0 & 0 \\ 0 & 0.4747 & -0.1830 & 0 & 0 & 0 \\ -0.1856 & -0.1830 & 0.4098 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0.7278 & -0.5817 & 0 \\ 0 & 0 & 0 & -0.5817 & 1.7878 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1.0515 \end{pmatrix}$$

Comparison of bus and loop frames of references: For the IEEE 14-bus test system, impedance matrices are calculated in bus and loop frames of references.

Table 2.Diagonal elements of primitive impedance matrix 'Z_{bb}'.

Diagonal element	Impedance (per unit)
1,1	0.22949
2,2	0.25202
3,3	0.28380
4,4	0.29792
5,5	0.38773
6,6	0.29876
7,7	0.09028
8,8	0.55618
9,9	0.17615
10,10	0.20912
11,11	0.18564
12,12	0.22041
13,13	0.18296
14,14	0.20347
15,15	0.18368
16,16	0.06226
17,17	0.04117
18,18	0.14610
19,19	0.20886
20,20	0.11001

Table 3. Comparison of frames of references.

Impedance	Computation time (sec)	Memory space(bytes)
Bus frame of reference (Z_{bus})	0.006563	583110656
Loop frame of reference (Z_{loop})	0.003232	525647872

Fig. 3. Comparison of computation time.

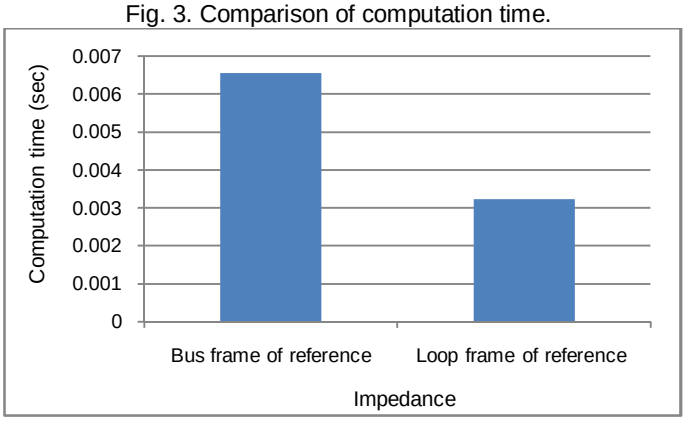
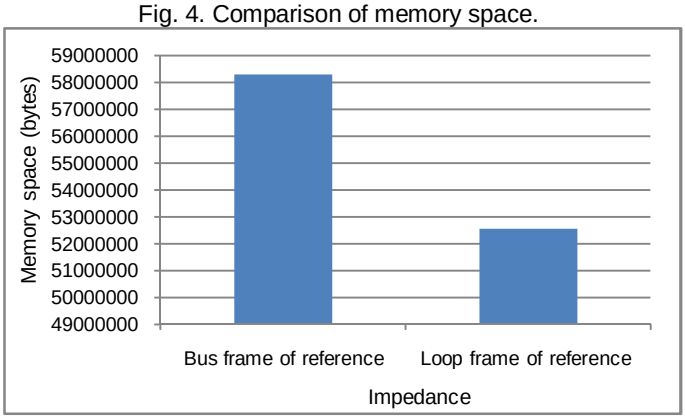


Fig. 4. Comparison of memory space.



In bus frame of reference, bus impedance matrix Z_{bus} is formulated by inverting bus admittance matrix (Y_{bus}). In loop frame of reference, loop impedance matrix Z_{loop} is calculated using graph theory. The results have proved that loop frame of reference can outperform the bus frame of reference with less computation time and memory. The computation time and memory space required in bus and loop frames of references are compared in Table 3 and illustrated in Fig. 3 and 4 respectively.

Conclusion

The loop impedance matrix Z_{loop}, developed based on the topological structure of power systems which can be used for the fault analysis of larger power systems. The loop impedance matrix is responsible for the variation between the loop current and branch current. Branches and links are responsible for the variation between the branch current and link current. Z_{loop} using loop incidence matrix '*C*' is calculated for IEEE 14-bus system through MATLAB. It is observed that conventional method Z_{bus} matrix size is large and hence the computational time is more compared to Z_{loop}. This study will help the researchers to perform fault analysis quickly with least matrix size using computer.

Acknowledgements

Authors thank the Principal and authorities of Government college of Technology, Coimbatore for providing necessary facilities to carry out this research work.

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